CLAIMS

[0073] What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A photosensor for use in a CMOS imaging device, said photosensor comprising:

a field oxide region formed in a substrate;

a doped layer of a first conductivity type formed in said substrate and adjacent said field oxide region;

a charge collection region formed in said doped layer; and

a charge storage capacitor connected to said charge collection region to store charge accumulated by said charge collection region, said charge storage capacitor overlying said field oxide region.

2. The photosensor according to claim 1, wherein said storage capacitor is a trench capacitor.

3. The photosensor according to claim 1, wherein said storage capacitor is a stacked capacitor.

4. The photosensor according to claim 1, wherein said storage capacitor is a metal capacitor.

5. The photosensor according to claim 1, wherein said storage capacitor is an HSG capacitor.

6. The photosensor according to claim 1, wherein said storage capacitor is a container capacitor.

7. The photosensor according to claim 1, wherein said storage capacitor is partially overlying said field oxide region.

8. The photosensor according to claim 1, wherein said storage capacitor is partially overlying over an active area of said photosensor.

9. The photosensor according to claim 1, wherein said storage capacitor is a flat plate capacitor.

10. The photosensor according to claim 9, wherein said storage capacitor is a flat plate capacitor including a first electrode, a second electrode and a dielectric layer between said first and second electrodes.

11. The photosensor according to claim 10, wherein said first and second electrodes are independently selected from the group consisting of doped polysilicon, hemispherical grained polysilicon, TiN, poly/WSix, polyTiSi_2, and poly/WNx/W.

12. The photosensor according to claim 1, further comprising a transistor for transferring charge accumulated in a second doped region of said second conductivity type adjacent to said charge collection region, wherein the gate of said transfer transistor is formed adjacent said second doped region and said charge collection region.

13. The photosensor according to claim 1, wherein an electrode of said storage capacitor is connected to the gate of said transfer transistor.

14. The photosensor according to claim 1, wherein said storage capacitor is connected to said charge collection region by a metal contact.

15. The photosensor according to claim 1 further comprising a reset transistor.

16. The photosensor according to claim 15, wherein an electrode of said storage capacitor is connected to said reset transistor.

17. The photosensor according to claim 1 further comprising a row select transistor.

18. The photosensor according to claim 17, wherein an electrode of said storage capacitor is connected to said row select transistor.

19. The photosensor according to claim 1 further comprising a diffusion region of said second conductivity type adjacent said transfer transistor.

20. The photosensor according to claim 19, wherein an electrode of said storage capacitor is connected to said diffusion region.

21. The photosensor according to claim 1 further comprising a source follower transistor.

22. The photosensor according to claim 21, wherein an electrode of said storage capacitor is connected to said source follower transistor.

23. The photosensor according to claim 1, further comprising a global shutter transistor.

24. The photosensor according to claim 23, wherein an electrode of said storage capacitor is connected to a gate of said global shutter transistor.

25. The photosensor according to claim 1, wherein said photosensor is a photogate.

26. The photosensor according to claim 1, wherein said photosensor is a photodiode.

27. The photosensor according to claim 1, wherein said photosensor is a photoconductor.

28. A photosensor for use in an imaging device formed in a single integrated circuit, said photosensor comprising:

a doped layer of a first conductivity type formed in a substrate;

a charge collection region formed in said doped layer;

a floating diffusion region for receiving charge from said charge collection region; and

a charge storage capacitor electrically connected to said floating diffusion region, said charge storage capacitor being formed at least partially over one of a field oxide region and an active area of said photosensor.

29. The photosensor according to claim 28, wherein said charge storage capacitor is formed fully over said field oxide region.

30. The photosensor according to claim 28, wherein said charge storage capacitor is formed fully over said active area.

31. The photosensor according to claim 28, wherein said charge storage capacitor is formed partially over said field oxide region.

32. The photosensor according to claim 28, wherein said charge storage capacitor is formed partially over said active area.

33. The photosensor according to claim 28, wherein said storage capacitor is a trench capacitor.

34. The photosensor according to claim 28, wherein said storage capacitor is a stacked capacitor.

35. The photosensor according to claim 28, wherein said storage capacitor is a metal capacitor.

36. The photosensor according to claim 28, wherein said storage capacitor is an HSG capacitor.

37. The photosensor according to claim 28, wherein said storage capacitor is a container capacitor.

38. The photosensor according to claim 28, wherein said storage capacitor is a flat plate capacitor.

39. The photosensor according to claim 28, wherein said storage capacitor is a flat plate capacitor including a first electrode, a second electrode and a insulating layer between said first and second electrodes.

40. The photosensor according to claim 39, wherein said floating diffusion region is connected to one of said first and second electrodes by an electrical contact.

41. The photosensor according to claim 39, wherein one of said first and second electrodes is further connected to a gate of a transfer transistor.

42. The photosensor according to claim 39, wherein said first and second electrodes are independently selected from the group consisting of doped polysilicon, hemispherical grained polysilicon, TiN, poly/WSix, polyTiSi$_2$, and poly/WNx/W.

43. The photosensor according to claim 28, wherein said first conductivity type is p-type, and said second conductivity type is n-type.

44. The photosensor according to claim 28, further comprising a source follower transistor for outputting charge accumulated in said floating diffusion region which has been transferred to said floating diffusion region, wherein the gate of said source follower transistor is formed adjacent said floating diffusion region.

45. The photosensor according to claim 44, wherein an electrode of said storage capacitor is further connected to the gate of said source follower transistor.

46. The photosensor according to claim 28 further comprising a reset transistor.

47. The photosensor according to claim 46, wherein an electrode of said storage capacitor is further connected to a gate of said reset transistor.

48. The photosensor according to claim 28 further comprising a global shutter transistor.

49. The photosensor according to claim 48, wherein an electrode of said storage capacitor is further connected to a gate of said global shutter transistor.

50. The photosensor according to claim 28, wherein said photosensor is used in a CMOS imager.

51. A photosensor for use in an imaging device, said photosensor comprising:

a field oxide region formed in a substrate;

a doped layer of a first conductivity type formed in said substrate and adjacent said field oxide region;

a charge collection region formed in said doped layer;

a first doped region of a second conductivity type formed in said doped layer adjacent said charge collection region; and

a first storage capacitor formed over said substrate adjacent said first doped region and connected to said first doped region to store charge collected in said charge collection region, said storage capacitor being formed at least partially over at least one of said field oxide region and an active area of said photosensor;

a transferred charge region for receiving charge from said charge collection region; and

a second storage capacitor connected to said transferred charge region.

52. The photosensor according to claim 51, wherein said second storage capacitor is formed at least partially over at least one of said field oxide region and said active area.

53. The photosensor according to claim 51, wherein said first and second capacitors are formed entirely over said field oxide region.

54. The photosensor according to claim 51, wherein said first and second capacitors are formed entirely over said active area.

55. The photosensor according to claim 51, wherein said first and second capacitors are independently selected from the group consisting of a trench capacitor, a stacked capacitor, a metal capacitor, an HSG capacitor, a container capacitor and a flat plate capacitor.

56. The photosensor according to claim 51, wherein said first capacitor is a flat capacitor including a first electrode, a second electrode and a dielectric layer between said first and second electrodes.

57. The photosensor according to claim 51, wherein said second capacitor is a flat capacitor including a first electrode, a second electrode and a dielectric layer between said first and second electrodes.

58. The photosensor according to claim 51, wherein said first conductivity type is p-type, and said second conductivity type is n-type.

59. The photosensor according to claim 51 further comprising a reset transistor.

60. The photosensor according to claim 59, wherein at least an electrode of said first and second storage capacitors is further connected to a gate of said reset transistor.

61. The photosensor according to claim 51 further comprising a source follower transistor for outputting charge accumulated in said transferred charge region which has been transferred to said transferred charge region, wherein the gate of said source follower transistor is formed adjacent said transferred charge region.

62. The photosensor according to claim 61, wherein at least an electrode of said first and second storage capacitors is further connected to the gate of said source follower transistor.

63. The photosensor according to claim 51 further comprising a row select transistor.

64. The photosensor according to claim 63, wherein at least an electrode of said first and second storage capacitors is further connected to a gate of said row select transistor.

65. The photosensor according to claim 51 further comprising a global shutter transistor.

66. The photosensor according to claim 65, wherein at least an electrode of said first and second storage capacitors is further connected to a gate of said global shutter transistor.

67. The photosensor according to claim 51, wherein at least an electrode of said first and second storage capacitors is further connected to said first doped region.

68. The photosensor according to claim 51, wherein at least an electrode of said first and second storage capacitors is further connected to said transferred charge region.

69. The photosensor according to claim 51, wherein said photosensor is used in a CMOS imager.

70. The photosensor according to claim 51, wherein said photosensor is a photogate.

71. The photosensor according to claim 51, wherein said photosensor is a photoconductor.

72. The photosensor according to claim 51, wherein said photosensor is a photodiode.

73. A CMOS imager system comprising:

(i) a processor; and

(ii) a CMOS imaging device coupled to said processor, said CMOS imaging device comprising:

a doped layer of a first conductivity type formed in a substrate and adjacent a field oxide region;

a charge collection region formed in said doped layer;

a first doped region of a second conductivity type formed in said doped layer adjacent said charge collection region; and

a charge storage capacitor formed entirely over said field oxide region.

74. The system according to claim 73, wherein said first conductivity type is p-type, and said second conductivity type is n-type.

75. The system according to claim 73, wherein said storage capacitor is a trench capacitor.

76. The system according to claim 73, wherein said storage capacitor is a stacked capacitor.

77. The system according to claim 73, wherein said storage capacitor is a metal capacitor.

78. The system according to claim 73, wherein said storage capacitor is an HSG capacitor.

79. The system according to claim 73, wherein said storage capacitor is a container capacitor.

80. The system according to claim 73, wherein said storage capacitor is a flat plate capacitor.

81. The system according to claim 73, further comprising a second doped region of a second conductivity formed in said doped layer adjacent a portion of said charge collection region and opposite said first doped region.

82. The system according to claim 73, further comprising a transfer transistor for transferring charge accumulated in said second doped region to a third doped region of said second conductivity type formed in said doped layer of said first conductivity type, wherein the gate of said transfer transistor is formed adjacent said second doped region.

83. The system according to claim 82, wherein an electrode of said storage capacitor is further connected to the gate of said transfer transistor.

84. The system according to claim 73, further comprising a source follower transistor for outputting charge accumulated in said third doped region which has been transferred to said third doped region, wherein the gate of said source follower transistor is formed adjacent said third doped region.

85. The system according to claim 84, wherein an electrode of said storage capacitor is further connected to the gate of said source follower transistor.

86. The system according to claim 73, further comprising a reset transistor.

87. The system according to claim 86, wherein an electrode of said storage capacitor is further connected to a gate of said reset transistor.

88. The system according to claim 73, further comprising a global shutter transistor.

89. The system according to claim 88, wherein an electrode of said storage capacitor is further connected to a gate of said global shutter transistor.

90. A method of forming a CMOS imager having improved charge storage comprising the steps of:

providing a semiconductor substrate having a doped layer of a first conductivity type;

forming a first doped region of a second conductivity type in said doped layer, said first doped region being adjacent a field oxide region;

forming a charge storage capacitor overlying entirely over at least one of said field oxide region and an active area of said CMOS imager; and

forming a contact between said first doped region and said charge storage capacitor.

91. The method according to claim 90, wherein said charge storage capacitor is formed entirely over said field oxide region.

92. The method according to claim 90, wherein said charge storage capacitor is formed entirely over said active area.

93. The method according to claim 90, wherein said charge storage capacitor is formed by:

forming a first conductive layer over said substrate including said field oxide region;

forming a dielectric layer over said first conductive layer; and

forming a second conductive layer over said dielectric layer.

94. The method according to claim 93, wherein said first and second conductive layers are independently selected from the group consisting of doped polysilicon, hemispherical grained polysilicon, TiN, poly/WSix, polyTiSi$_2$, and poly/WNx/W.

95. The method according to claim 90, further comprising forming an element of said CMOS imager simultaneously with forming said storage capacitor.

96. The method according to claim 95, wherein said element is a transistor gate.

97. The method according to claim 96, further comprising connecting an electrode of said storage capacitor to said transistor gate.

98. The method according to claim 95, wherein said element is a transfer gate.

99. The method according to claim 98, further comprising connecting an electrode of said storage capacitor to said transfer gate.

100. The method according to claim 95, wherein said element is a source follower gate.

101. The method according to claim 100, further comprising connecting an electrode of said storage capacitor to said source follower gate.

102. The method according to claim 95, wherein said element is a gate of a global shutter transistor.

103. The method according to claim 102, further comprising connecting an electrode of said storage capacitor to said gate of said global shutter transistor.

104. The method according to claim 90, further comprising:

forming a second doped region of said second conductivity type in the doped layer spaced from said first doped region to transfer charge from a charge collection area;

forming a third doped region of said second conductivity type in the doped layer spaced from said second doped region wherein said third doped region effectuates the transfer of charge to a readout circuit; and

forming a fourth doped region of said second conductivity type in the doped layer spaced from said third doped region wherein said fourth doped region is a drain for a reset transistor for said CMOS imager.

105. The method according to claim 104, wherein said first conductivity type is p-type, and said second conductivity type is n-type.

106. The method according to claim 104, further comprising forming a photogate over said doped layer between said first and second doped regions.

107. The method according to claim 106, further comprising connecting an electrode of said storage capacitor to said photogate.

108. A method of forming a CMOS imager having improved charge storage comprising the steps of:

providing a semiconductor substrate having a doped layer of a first conductivity type;

forming a field oxide region within said semiconductor substrate;

forming a first conductive layer over said field oxide region and said substrate;

forming an insulating layer over said first conductive layer;

forming a second conductive layer over said insulating layer;

patterning said first conductive layer, said insulating layer and said second conductive layer to form a storage capacitor and an electrical element of said CMOS imager, wherein said storage capacitor is formed entirely over and in contact with said field oxide region.

109. The method according to claim 108, further comprising:

forming a first doped region of a second conductivity type in said doped layer and adjacent said field oxide region;

forming a second doped region of said second conductivity type in said doped layer spaced from said first doped region;

forming a third doped region of said second conductivity type in said doped layer spaced from said second doped region and adjacent said electrical element; and

forming a fourth doped region of said second conductivity type in said doped layer spaced from said third doped region.

110. The method according to claim 109, wherein said first conductivity type is p-type, and said second conductivity type is n-type.

111. The method according to claim 109, wherein said first doped region, said second doped region, said third doped region and said fourth doped region are doped at a dopant concentration of from about $1x10^{15}$ ions/cm^2 to about $1x10^{16}$ ions/cm^2.

112. The method according to claim 108, wherein said electrical element is a transistor gate.

113. The method according to claim 112, further comprising connecting an electrode of said storage capacitor to said transistor gate.

114. The method according to claim 108, wherein said electrical element is a reset transistor gate.

115. The method according to claim 114, further comprising connecting an electrode of said storage capacitor to said reset transistor gate.

116. The method according to claim 108, wherein said electrical element is a source follower transistor gate.

117. The method according to claim 116, further comprising connecting an electrode of said storage capacitor to said source follower transistor gate.

118. The method according to claim 108, wherein said electrical element is a row select transistor gate.

119. The method according to claim 118, further comprising connecting an electrode of said storage capacitor to said row select transistor gate.

120. The method according to claim 108, wherein said electrical element is a gate of a global shutter transistor.

121. The method according to claim 120, further comprising connecting an electrode of said storage capacitor to said gate of said global shutter transistor.